ABSTRACT

According to one exemplary embodiment, a BiFET situated on a substrate comprises an emitter layer segment situated over the substrate, where the emitter layer segment comprises a semiconductor of a first type. The HBT further comprises a first segment of an etch stop layer, where the first segment of the etch stop layer comprises InGaP. The BiFET further comprises a FET situated over the substrate, where the FET comprises source and drain regions, where a second segment of the etch stop layer is situated under the source and drain regions, and where the second segment of the etch stop layer comprises InGaP. The FET further comprises a semiconductor layer of a second type situated under the second segment of the etch stop layer. The etch stop layer increases linearity of the FET and does not degrade electron current flow in the HBT.